I claim:

1. An integrated circuit comprising:

A. a semiconductor substrate;

B. functional circuits formed on the substrate;

C. bond pads formed on the substrate and connected to the functional circuits;

D. parallel scan paths circuits formed on the substrate and connected to the functional circuits, each of the parallel scan path circuits having a serial input and a serial output;

E. at least one scan distributor circuit having a serial input connected to a first bond pad and having parallel outputs, each parallel output being connected to an input of a parallel scan path circuit; and

F. at least one scan collector circuit having a serial output connected to a second bond pad separate from the first bond pad and having parallel inputs, each input being connected to an output of a respective parallel scan circuit connected to the at least one scan distributor circuit.

2. The integrated circuit of claim 1 in which the scan distributor circuit is a serial input, parallel output circuit and the scan collector circuit is a parallel input and serial output circuit.

3. The integrated circuit of claim 1 including a controller connected to bond pads and to the scan distributor circuit, the scan path circuits and the scan collector circuit.

4. The integrated circuit of claim 1 in which the scan distributor circuit includes a serial output and the scan collector circuit includes a serial input and including at least another scan distributor circuit having a serial input coupled to the serial output of the scan distributor by a multiplexer and including at least another scan collector circuit having a serial output coupled to the serial input of the scan collector by a demultiplexer.

5. An integrated circuit comprising:

A. a semiconductor substrate;

B. functional circuits formed on the substrate;

C. bond pads formed on the substrate and connected to the functional circuits;

D. a first group of parallel scan paths circuits formed on the substrate and connected to the functional circuits, each of the first group of parallel scan path circuits having a serial input and a serial output;

E. a first scan distributor circuit having a serial input connected to a first bond pad, a serial output and parallel outputs, each parallel output being connected to an input of a parallel scan path circuit of the first group;

F. a first scan collector circuit having a serial output connected to a second bond pad separate from the first bond pad, a serial input and parallel inputs, each parallel input being connected to an output of a respective parallel scan circuit of the first group;

G. core circuits, separate from the functional circuits, formed on the substrate;

H. a second group of parallel scan paths circuits formed on the substrate and connected to the core circuits, each of the second group of parallel scan path circuits having a serial input and a serial output;

I. a second scan distributor circuit having a serial input coupled to the serial output of the first scan distributor and parallel outputs, each parallel output being connected to an input of a parallel scan path circuit of the second group; and

J. a second scan collector circuit having a serial output coupled to the serial input of the first scan collector and parallel inputs, each parallel input being connected to an output of a respective parallel scan circuit of the second group.

6. The integrated circuit of claim 5 including a multiplexer selectively coupling the serial output of the first scan distributor circuit to the serial input of the second scan distributor circuit and a demultiplexer selectively coupling the serial output of the second scan collector to the serial input of the first scan collector circuit.

7. The integrated circuit of claim 1 in which the serial output of the first scan distributor circuit is connected to the serial input of the second scan distributor and the serial output of the second scan collector is connected to the serial input of the first scan collector.

8. The integrated circuit of claim 1 including plural scan distributor circuits connected in series to the first bond pad and plural scan distributor circuits connected in series to the second bond pad.

9. The integrated circuit of claim 1 including a third scan distributor circuit having a serial input and a third

scan collector circuit having a serial output and multiplexer circuits selectively connecting the serial output of the first scan distributor to the serial inputs of the second and third scan distributors and selectively connecting the serial outputs of the second and third scan collectors to the serial input of the first scan collector.

10. A process of testing an integrated circuit comprising:

A. receiving test stimulus data on one bond pad on the integrated circuit;

B. distributing the received test stimulus data to plural parallel scan paths on the integrated circuit; and

C. applying the test stimulus data in the parallel scan circuits to functional circuits on the integrated circuit.

11. The process of claim 10 in which the distributing includes performing a serial to parallel conversion.

12. A process of testing an integrated circuit comprising:

A. receiving test response data in parallel scan circuits from functional circuits on the integrated circuit;

B. collecting the received test response data from the parallel scan circuits; and

C. applying the collected test response data to one bond pad on the integrated circuit.

13. The process of claim 12 in which the collecting includes performing a parallel to serial conversion.

14. An integrated circuit comprising;

A. a semiconductor substrate;

B. functional circuits formed on the substrate;

C. parallel scan path circuits formed on the substrate and connected to the functional circuits, each of the parallel scan path circuits having a serial input and a serial output;

D. at least one scan distributor circuit having a serial input for receiving test data and having parallel outputs, each parallel output being connected to an input of a parallel scan path circuit; and

E. at least one scan collector circuit having a serial output for transmitting test data and having parallel inputs, each input being connected to an output of a respective parallel scan circuit connected to the at least one scan distributor circuit.

15. The integrated circuit of claim 14 in which the functional circuits include combinational logic.